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Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR(S): **MCBRIDE, Brian E.**

FOR: **CELL STREAM REPLICATING DEVICE**

Enclosed are:

☐ ___5___ sheet(s) of ☑ formal or ☐ informal drawings.

☑ An assignment of the invention to: **NEWBRIDGE NETWORKS CORPORATION**

☐ A verified statement to establish small entity status under 37 C.F.R. 1.9 and 37 C.F.R. 1.27.

☐ Information Disclosure Statement.

☑ Executed (☐ Un-executed) Declaration and Power of Attorney.

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FOR:	No. Filed	No. Extra	RATE	FEE	RATE	FEE
BASIC FEE				$380		$760
TOTAL CLAIMS	46 -20=	26	x9	$	x18	$468
INDEPENDENT CLAIMS	12 -3=	9	x39	$	x78	$702
MULTIPLE DEPENDENT CLAIMS PRESENTED			+130	$	+260	$
If the difference in Col. 1 is less than zero, enter "0" in Col. 2			TOTAL	$	TOTAL	$1930.00

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Any patent application processing fees under 37 C.F.R. § 1.17.
Any filing fees under 37 C.F.R. § 1.16 for presentation of extra claims.

BLAKE, CASSELS & GRAYDON

Date: March 2, 1999

By: Alex Borat

Registration No. 43,372

CELL STREAM REPLICATING DEVICE

Field of Invention

The invention generally relates to testing equipment for digital data communication devices, and more particularly to a device which generates a plurality of data traffic streams based on a single traffic stream.

Background of Invention

Testing of packet/cell based data communication devices, such as asynchronous transfer mode (ATM) based network nodes, is becoming more important as data communication technologies mature. This is because the majority of data communications devices implement standard protocols, and thus their functionality is more or less equivalent. Hence, a distinguishing factor between such devices is their performance under known, real world conditions, which customers often examine in order to base their purchase decisions. The desire for performance testing requirements can be seen in the standards setting bodies and industry associations such as the International Telecommunications Union (ITU), the Internet Engineering Task Force (IETF) and the ATM Forum, where numerous performance testing specifications are currently in the process of being drafted.

Performance testing requires the use of standardized traffic patterns on all input ports to a data communication device so that different devices may be tested under the same traffic conditions. Unfortunately, the costs are enormous with the present practice of using a test generator for each port. The average per port cost of good ATM traffic pattern generator is quite high, so the cost to test a device having a large number of ports can be quite large. For example, some ATM switches have 92 ports thereby requiring 92 test generators at a cost of several millions of dollars in order to test the

switch. Due to the large testing costs, customers do not test all ports at once and thus cannot obtain a true evaluation of the performance of a device for comparison against others.

Accordingly, there exists a need to carry out performance testing in data communication devices in a cost effective manner.

Summary of Invention

According to one aspect of the invention, there is provided a method of generating digital traffic for use in testing a multi-port communications device. This method comprises the steps of generating a reference pattern defining the digital traffic, such as provided by a known test generator; and generating a plurality of traffic streams from the reference pattern, whereby the plural traffic streams are used for loading respective input ports of the communications device. In the preferred embodiment, respective phase delays are introduced between the plural traffic streams in order to mimic real world conditions on the input ports of the communications device using only one test generator whilst respecting any statistical multiplexing advantages provided the device.

According to another aspect of the invention, there is provided a method of loading a multi-port communications device with digital traffic. This method comprises the steps of: generating the digital traffic; and providing plural streams of the generated digital traffic to respective input ports of the communications device with phase delays.

According to another aspect of the invention, there is provided a method of loading a multi-port communications device with digital traffic. This method comprises the steps of: generating a plurality of identical digital traffic streams; and providing the identical streams to respective input ports of the communications device with phase delays.

According to another aspect of the invention, a digital data stream replicating device is provided comprising an input port for receiving a continuous digital data stream at an input transmission rate; broadcast means for replicating the input digital data stream N times; N output ports for transmitting each such replicated digital data stream through a separate output port at an output transmission rate at least equal to the input transmission rate; and delay means for introducing a relative delay for each said output digital data stream with respect to the input digital data stream such that the output streams are similar to the input stream but out of phase with one another. Use of such a device makes it possible to test a multi-port digital data communications device such as an ATM network switch using only one performance test generator whilst respecting the statistical multiplexing advantages of the multi-port digital data communications device.

In the preferred embodiment, the replicating device includes means for introducing empty data blocks into the output digital data stream when the output transmission rate of the corresponding output port is greater than the input transmission rate.

In the preferred embodiment, the delay means comprises a memory and N first-in first-out logical buffers established therein. Each logical buffer is associated with a separate replicated digital data stream, wherein data blocks associated with each

logical buffer are forwarded to the corresponding output port only when the logical buffer is full such that the relative delay encountered by the replicated cell stream corresponds to the length of the logical buffer. The delay means for each replicated output digital data stream may also include the output transmission rate of the corresponding output port, whereby the relative delay encountered by the replicated digital data stream corresponds to the transmission rate of the corresponding output port.

The above-mentioned logical buffers may be established by copying each input data block into different physical buffers organized in the memory. Alternatively, the logical buffers may be established by copying each input data block into one physical buffer and maintaining a separate pointer to the physical buffer for each logical buffer.

In the preferred embodiments, the input and output digital data streams are ATM cell streams.

Brief Description of Drawings

The foregoing and other aspects of the invention will become more apparent from the following description of the preferred embodiments thereof and the accompanying drawings which illustrate, by way of example, the principles of the invention. In the drawings:

Figure 1 is functional block diagram of a cell stream replicating device according to the preferred embodiment;

Figure 2 is a timing diagram illustrating output cell streams which are delayed with respect to an input cell stream;

Figure 3A and 3B are system block diagrams of two implementations of the cell stream replicating device according to the preferred embodiment; and

Figure 4 is a timing diagram illustrating output cell streams which are delayed with respect to the input cell stream in situations where the output transmission rate is greater than the input transmission rate.

Detailed Description of Preferred Embodiments

The functional block diagram of Figure 1 illustrates a cell stream replicating device 10 according to the preferred embodiment which is connected between an ATM traffic generator 12 and a multiple input port ATM data communications device 14, such as an ATM cell switching device. The ATM traffic generator 12 produces an ATM cell stream, such as shown at ref. no. 54 in Figure 2, on physical interface/line 16 (Figure 1). The cell stream 54 carries a traffic pattern used for testing purposes such as performance testing. As noted from Figure 2, the ATM cell stream 54 is "continuous" in the sense that even if there is no user information or data payload being carried by the cell stream at any given point in time (i.e. other than the ATM control information encapsulated in the cell header which is required for the functioning of the cell stream itself), the ATM traffic generator 12 generates idle or unassigned ATM cells 53 as known in the art, such that there are no gaps or discontinuities in the cell stream. Test generator 12 is commercially available from a variety of sources, including the Interwatch 95000 model by GN Nettest and the AX4000 model Adtech.

The cell stream replicating device 10 includes an input port 18 for receiving cell stream 54 on line 16 at the transmission rate thereof. (Cell stream 54 is thus an input to the replicating device 10). A broadcast means 20 replicates cell stream 54 N times on N different outputs 22. A delay means 24 introduces a relative delay for each replicated

cell stream with respect to cell stream 54. The device 10 also includes N output ports 28 for transmitting the N copies or replicas of cell stream 54, each through a separate output port, at an output transmission rate equal to the transmission rate of cell stream 54.

In the preferred embodiment, the delay means 24 comprises N logical first-in first-out (FIFO) buffers 26, as explained in greater detail below, in conjunction with a scheduling means 25. The broadcast means 20 associates or stores each cell of cell stream 54 with each of the logical FIFO buffers 26, as explained in greater detail below. Scheduling means 25 forwards the lead cell in a given logical buffer 26 to the corresponding output port 28 only when that logical buffer is full. Therefore, the relative delay encountered by each replicated cell stream on outputs 22 with respect to cell stream 54 on input line 16 corresponds to the length, in terms of the number of cells, of the corresponding logical buffer 26. More specifically, the average delay encountered by a given replicated cell stream is equal to:

$$delay_{avg} = \frac{1}{Buffer\,Length * Output\,Transfer\,Rate} \quad (1)$$

This is illustrated in the timing diagram of Figure 2 where three (for example) replicated output streams, respectively designated by ref. nos. 56, 58 and 60, are shown. The delay means produces relative delays or phase delays t_b, t_c, and t_d in the three replicated cell streams 56, 58 and 60 relative to cell stream 54, the magnitude of which are dependent upon the respective lengths of the corresponding logical buffers 26. It will thus be seen from Figure 2 that the traffic pattern of each output cell stream is equivalent to the traffic pattern of cell stream 54; except for being out of phase with one another. This results in well defined traffic patterns on the N outputs 28, which do not occur simultaneously, thereby mimicking real world conditions on the N input ports of

the ATM device 14 using only one traffic test generator 12. It will be appreciated that this phasing respects the statistical multiplexing advantages of ATM devices, as the test data traffic, in particular ATM cells associated with variable bit rate (VBR) service class virtual connections, arrive at the input ports of an ATM device in a more random fashion. Statistical multiplexing devices are designed to take advantage of burstiness and randomness behaviour of typical data traffic, and the introduction of respective delays in the multiple replicated test streams attempts to mimic this behaviour.

Figure 3A is a system block diagram illustrating a first system for carrying out the preferred embodiment in practice. In this system, the cell stream replicating device 10 comprises a microprocessor 30 and an associated memory 32 which may be internal to (e.g., a high speed cache memory) or external of the microprocessor 30. The input port 18 is a serial port which converts a bit stream into corresponding word data readable by the microprocessor 30. The serial port 13 is connected to the microprocessor 30 via an interrupt signal 34. The microprocessor is also connected to output ports 28 through various means well known in the art. In this case, the output ports 28 are serial ports which convert word data provided by the microprocessor 30 into a serial bit stream.

In the illustrated embodiment, memory 32 is organized into N physical FIFO buffers 27 such that each logical buffer 26 corresponds to one of the physical buffers 27. The microprocessor 32 implements the broadcast means 20, a portion of the delay means 24, and the scheduling means 25 by executing a program which, upon receipt of a new cell from the input port 18, copies the new cell to each physical buffer 27. The program also determines when any of the physical buffers 27 are full, and, for those buffers which are full, forwards the lead cells stored therein to the corresponding output ports 28. A housekeeping function of the program maintains each physical buffer by discarding cells which have been transmitted. For example, the physical buffers 27

may be constructed as linked lists, the lead elements of which are discarded when the data is forwarded to the output ports 28.

Figure 3B illustrates a second system for carrying out the preferred embodiment in practice, which uses the same hardware shown in Figure 3A. In this system, the memory 32 is organized so that there is only one physical buffer 27' into which all cells received from the input port 18 are stored. However, a program executing on the microprocessor 30 maintains a pointer 40 and buffer length register 42 in respect of each logical buffer 26 (i.e., there are N sets of registers 40 and 42). The pointer 40 associated with each logical buffer 26 may point to different cells stored in the physical buffer 27' as illustrated. In each case, the pointer 40 points to the first cell of the respective logical buffer. The program determines when each logical buffer 26 is full based on a comparison of the corresponding buffer length register 42 against the distance or length of the corresponding pointer 40 to the last cell 50 stored in the physical buffer 27. If the results of the comparison indicate that a given logical buffer 26 is full, the microprocessor 30 copies the cell pointed to by the corresponding pointer 40 to the corresponding output port 28. A housekeeping function of the program maintains the physical buffer 27' in order to add new cells received from the input port 18 and to delete cells which have already been transmitted to all of the output ports 28. For example, the physical buffer 27' may be constructed as a linked list data structure. In such a case, as illustrated for instance in Figure 3B where all of the pointers 40 are pointing to a cell beyond a first cell 49 in the physical buffer 27', the housekeeping function recognizes that cells such as cell 49 have already been transmitted on all the output ports 28 and thus deletes such cells from the linked list. Further details regarding implementation of multiple logical buffers using a single physical buffer may be found, for instance, in US Patent No. 5,528,588 to Bennett et al., which is incorporated herein by reference.

In the preferred embodiment the output ports 28 transmit data at a rate equal to the transmission rate of the input cell stream (line 16). However, it will be readily recognized from equation (1) that the average delay experienced by each replicated cell stream can also be varied by modifying the output transfer rate of the output port 28, provided the transmission rate of any given output port is greater then the transmission rate of (input) cell stream 54. In this embodiment, the output ports 28 are more sophisticated ATM segmentation and reassembly (SAR) devices. Such a device is capable of attaching header information to data destined for transport over an ATM link, and is capable of inserting idle or unassigned cells (i.e., cells not carrying any payload which are designed to be discarded by the receiving side) when there is no data to be transmitted. It will be appreciated that if the output ports 28 transmit at a rate greater than the transmission rate of (input) cell stream 54, it is necessary to insert idle cells in the output cell streams in order to perform a cell rate decoupling or speed matching function. An example of this phenomenon is shown in Figure 4, where the vertical axis of the timing diagram represents the bandwidth or transmission rate of any given cell stream. In the illustrated example, replicated output cell stream 58' has a transmission rate, and hence bandwidth occupancy, which is twice that of cell stream 54. Thus, for instance, data payload A is transmitted in the replicated cell stream 58' in half the time that the data payload A is transmitted in cell stream 54. This necessitates the inclusion of an empty cell 62 between data payload A and the following adjacent data payload B in cell stream 58'.

In order to accommodate this function, the scheduling means 25 according to this alternative embodiment forwards the data payload of the ATM cells stored in the logical buffers 26 to the SAR interface devices which function as output ports 18 (as opposed to forwarding the entire ATM cell, inclusive of header, to the serial ports of the preferred embodiment). In addition, the modified scheduling means 25 sends the channel

and other control information stored in the ATM cell headers (of cells associated with the logical buffers 26) separately to the SAR interface devices, in accordance with the particular interface protocols thereof.

The above-described embodiments of the invention have made reference to fixed length ATM cells and ATM cells streams. However, those skilled in the art will appreciate that the invention may be applied more generically to other types of continuous digital data streams including others which are formatted into discrete data blocks or packets, such as TDM and SONET. Furthermore, although the test traffic generation function and the traffic replicating function are implemented by separate entities in the above description, both of these functions may be provided within the same entity. Similarly, other modifications and variations may be made to the embodiments disclosed herein without departing from the spirit of the invention.

Claims

1. A method of generating digital traffic for use in testing a multi-port communications device, said method comprising the steps of:

generating a reference pattern defining the digital traffic; and

generating a plurality of traffic streams from the reference pattern, whereby the plural traffic streams are used for loading respective input ports of the communications device.

2. The method as claimed in claim 1, further including the step of introducing respective phase delays between said plural traffic streams.

3. The method according to claim 2, wherein the communications device effects statistical multiplexing.

4. The method according to claim 3, wherein the plural traffic streams are continuous digital data streams.

5. The method according to claim 4, wherein the plural traffic streams are ATM cell streams.

6. A method of loading a multi-port communications device with digital traffic, said method comprising the steps of:

generating the digital traffic; and

providing plural streams of the generated digital traffic to respective input ports of the communications device with phase delays.

7. The method according to claim 6, wherein the communications device effects statistical multiplexing.

8. A method of loading a multi-port communications device with digital traffic, said method comprising the steps of:

generating a plurality of identical digital traffic streams; and

providing the identical streams with phase delays to respective input ports of the communications device.

9. The method according to claim 8, wherein the communications device effects statistical multiplexing.

10. A method of operating a digital traffic replicating device, comprising the steps of:

receiving a digital traffic stream;

generating a plurality of output digital traffic streams from the received digital traffic, wherein the output streams include respective phase delays.

11. The method according to claim 10, wherein the output streams have traffic patterns which are replicas of the received digital traffic stream.

12. The method according to claim 8, wherein the communications device effects statistical multiplexing.

13. Apparatus for generating digital traffic for use in testing a multi-port communications device, said apparatus comprising:

means for generating a reference pattern defining the digital traffic; and

means for generating a plurality of traffic streams from the reference pattern, whereby the plural traffic streams are used for loading respective input ports of the communications device.

14. The apparatus as claimed in claim 15, further including means for introducing respective phase delays between said plural traffic streams.

15. The apparatus according to claim 14, wherein the communications device effects statistical multiplexing.

16. The apparatus according to claim 15, wherein the plural traffic streams are continuous digital data streams.

17. The apparatus according to claim 16, wherein the plural traffic streams are ATM cell streams.

18. An apparatus for loading a multi-port communications device with digital traffic, said apparatus comprising:

means for generating the digital traffic; and

means for providing plural streams of the generated digital traffic to respective input ports of the communications device with phase delays.

19. The apparatus according to claim 18, wherein the communications device effects statistical multiplexing.

20. Apparatus for loading a multi-port communications device with digital traffic, said apparatus comprising:

means for generating a plurality of identical digital traffic streams; and

means for providing the identical streams to respective input ports of the communications device with phase delays.

21. The apparatus according to claim 20, wherein the communications device effects statistical multiplexing.

22. A digital data stream replicating device, comprising:

an input port for receiving an input continuous digital data stream at an input transmission rate;

broadcast means for replicating the input digital data stream N times;

N output ports for transmitting each such replicated digital data stream through a separate output port at an output transmission rate at least equal to the input transmission rate; and

delay means for introducing a relative delay for each said output digital data stream with respect to the input digital data stream.

23. The device according to claim 22, including means for introducing idle data blocks into the output digital data stream when the output transmission rate of the corresponding output port is greater than the input transmission rate.

24. The device according to claim 22, wherein the delay means comprises a memory and N first-in first-out logical buffers established therein, each logical buffer being associated with a separate replicated digital data stream, wherein data blocks associated with each logical buffer are forwarded to the corresponding output port only when the logical buffer is full such that the relative delay encountered by the replicated cell stream corresponds to the length of the logical buffer.

25. The device according to claim 23, wherein the delay means comprises a memory and N first-in first-out logical buffers established therein, each logical buffer being associated with a separate replicated digital data stream, wherein data blocks associated with each logical buffer are forwarded to the corresponding output port only when the logical buffer is full such that the relative delay encountered by the replicated digital data stream corresponds to the length of the logical buffer.

26. The device according to claim 25, wherein the delay means for each replicated output digital data stream comprises the output transmission rate of the corresponding output port, whereby the relative delay encountered by the replicated digital data stream corresponds to the transmission rate of the corresponding output port.

27 The device according to claim 24, wherein logical buffers are established by copying each input data block into different physical buffers organized in the memory.

28. The device according to claim 26, wherein logical buffers are established by copying each input data block into different physical buffers organized in the memory.

29. The device according to claim 24, wherein logical buffers are established by copying each input data block into one physical buffer and maintaining a separate pointer to the physical buffer for each logical buffer.

30. The device according to claim 26, wherein logical buffers are established by copying each input data block into one physical buffer and maintaining a separate pointer to the physical buffer for each logical buffer.

31. The device according to claim 24, wherein the input and output digital data streams are ATM cell streams.

32. The device according to claim 26, wherein the input and output digital data streams are ATM cell streams.

33. A digital data stream replicating device, comprising:

an input port for receiving a continuous digital data stream at an input transmission rate;

a memory;

N output ports, each having an output transmission rate equal to the input transmission rate;

processing means, connected between the input port and the N output ports, for establishing N first-in first-out logical buffers and associating each data block of the input digital data stream with each one of the N logical buffers, each logical buffer being associated with only one of the output ports; and

scheduling means for forwarding data blocks associated with a given logical buffer through the corresponding output port when the given logical buffer is full.

34. The device according to claim 33, wherein the length of each logical buffer is selected to achieve a relative delay between the input digital data stream and the corresponding replicated digital data stream generated at the corresponding output port.

35. The device according to claim 34, wherein the logical buffers are established by copying each input data block into different physical buffers organized in the memory .

36. The device according to claim 34, wherein the logical buffers are established by copying each input cell into one physical buffer and maintaining a separate pointer to the physical buffer for each logical buffer.

37. The device according to claim 34, wherein the input and output digital data streams are ATM streams.

38. A digital data stream replicating device, comprising:

an input port for receiving a continuous digital data stream at an input transmission rate;

a memory;

N output ports, each having an output transmission rate at least equal to the input transmission rate;

processing means, connected between the input port and the N output ports, for establishing N first-in first-out logical buffers and associating each data block of the input digital data stream with each one of the N logical buffers, each logical buffer being associated with only one of the output ports; and

scheduling means for forwarding data blocks associated with a given logical buffer through the corresponding output port when the given logical buffer is full.

39. The device according to claim 38, including means for introducing empty data blocks into the output digital data stream when the output transmission rate of the corresponding output port is greater than the input transmission rate.

40. The device according to claim 39, wherein the length of each logical buffer and the output transmission rate of the corresponding output port are selected to achieve

a relative delay between the input digital data stream and the corresponding replicated digital data stream generated at the corresponding output port.

41. The device according to claim 39, wherein the logical buffers are established by copying each input data block into different physical buffers organized in the memory .

42. The device according to claim 39, wherein the logical buffers are established by copying each input cell into one physical buffer and maintaining a separate pointer to the physical buffer for each logical buffer.

43. The device according to claim 39, wherein the input and output digital data streams are ATM streams.

44. A performance testing device, comprising:

a traffic generator for generating a continuous digital data stream;

an input port for receiving the continuous digital data stream at an input transmission rate;

broadcast means for replicating the input digital data stream N times;

N output ports for transmitting each such replicated digital data stream through a separate output port at an output transmission rate at least equal to the input transmission rate; and

delay means for introducing a relative delay for each said output digital data stream with respect to the input digital data stream.

45. A performance testing device, comprising:

a traffic generator for generating a continuous digital data stream;

an input port for receiving the continuous digital data stream at an input transmission rate;

a memory;

N output ports, each having an output transmission rate at least equal to the input transmission rate;

processing means, connected between the input port and the N output ports, for establishing N first-in first-out logical buffers and associating each data block of the input digital data stream with each one of the N logical buffers, each logical buffer being associated with only one of the output ports; and

scheduling means for forwarding data blocks associated with a given logical buffer through the corresponding output port when the given logical buffer is full.

46. The device according to claim 45, including means for introducing idle data blocks into the output digital data stream when the output transmission rate of the corresponding output port is greater than the input transmission rate.

ABSTRACT

The digital data stream (e.g. ATM cell stream) replicating device features an input port for receiving a continuous digital data stream at an input transmission rate; a broadcast mechanism for replicating the input digital data stream N times; N output ports for transmitting each such replicated digital data stream through a separate output port at an output transmission rate at least equal to the input transmission rate; and a delay mechanism for introducing a relative delay for each said output digital data stream with respect to the input digital data stream such that the output streams are identical but out of phase with one another. Use of such a device enables a multi-port digital data communications device such as an ATM network switch to be tested using only one (expensive) performance test generator whilst still respecting the statistical multiplexing advantages of the multi-port digital data communications device.

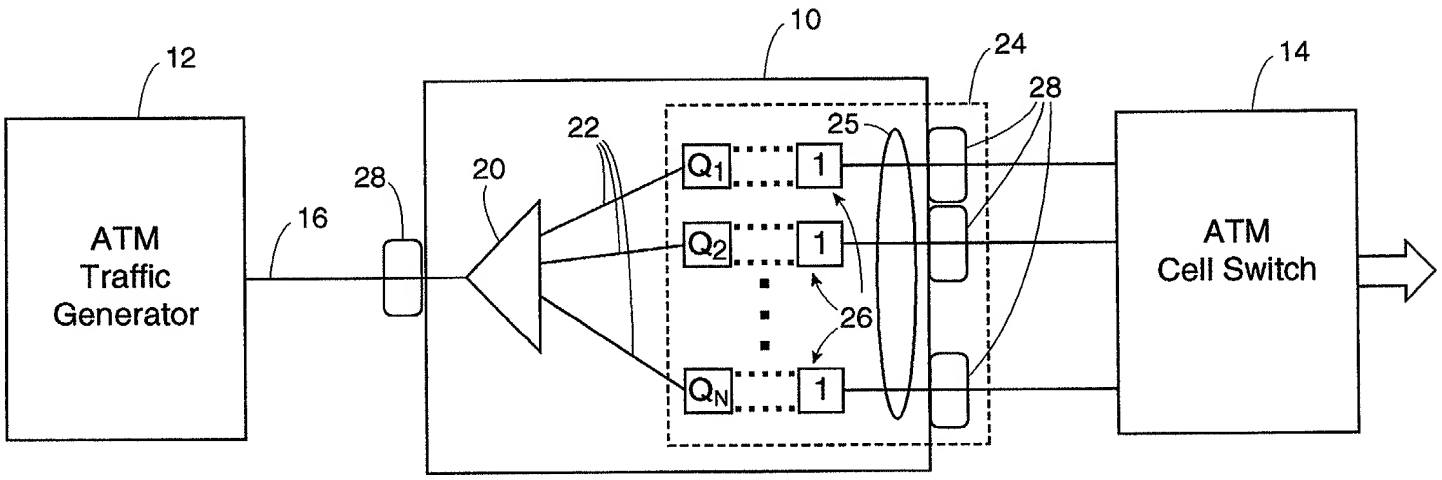


Figure 1

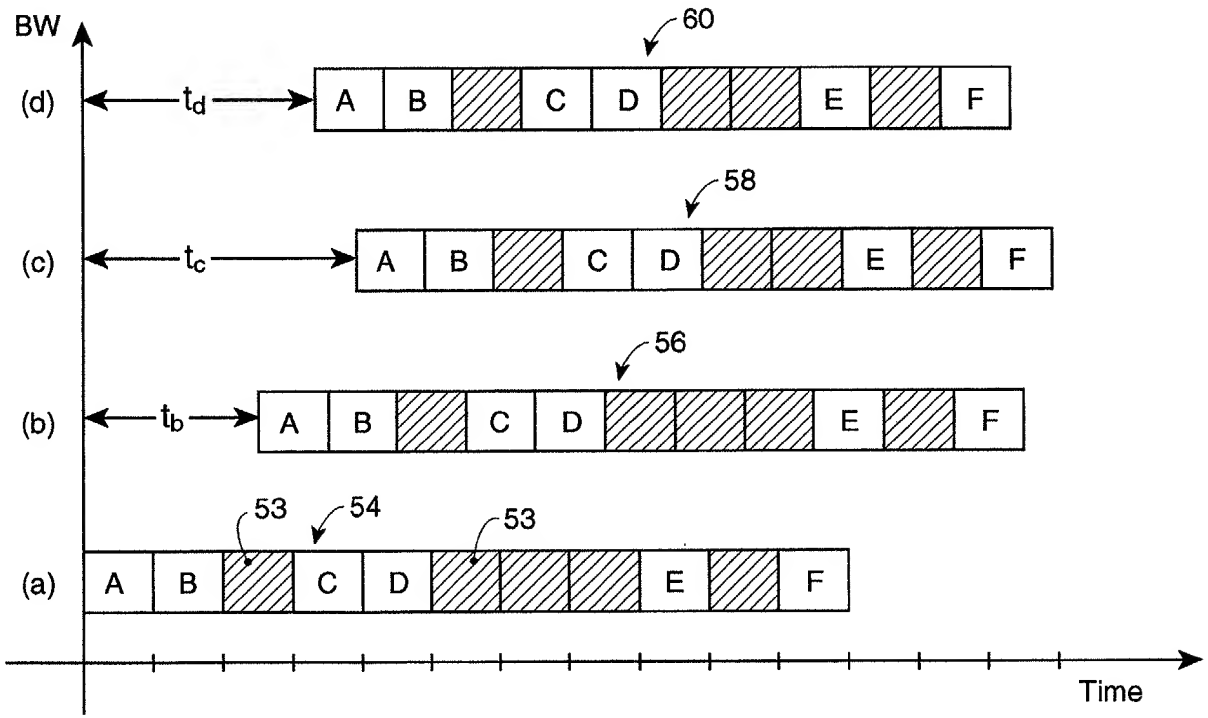


Figure 2

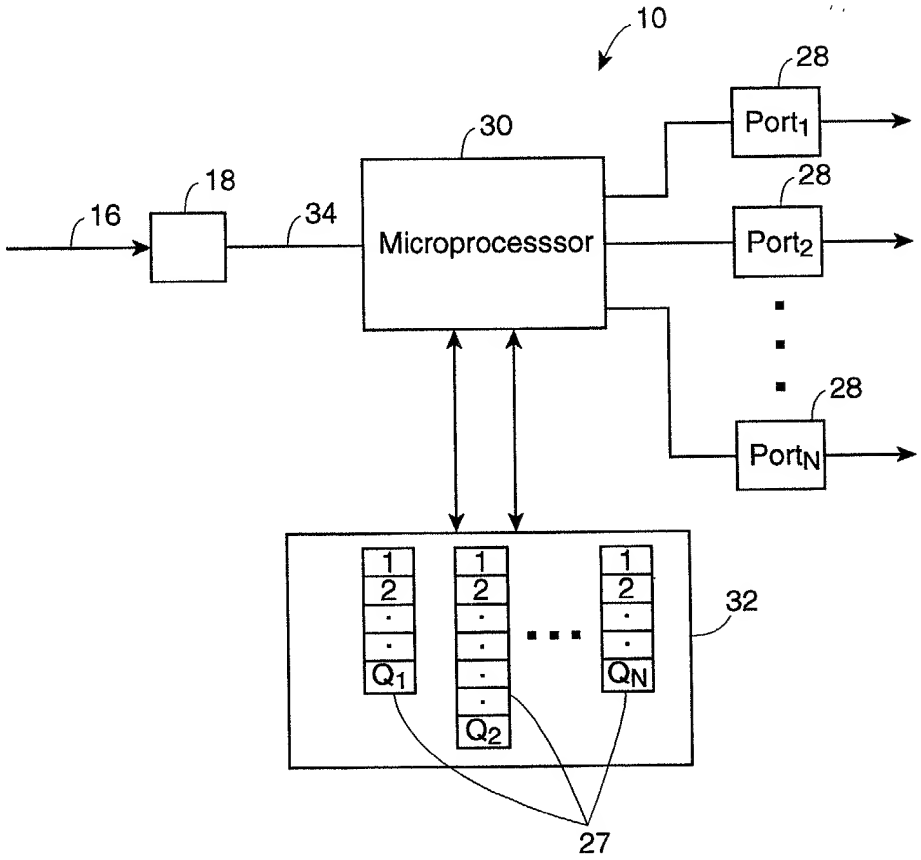


Figure 3A

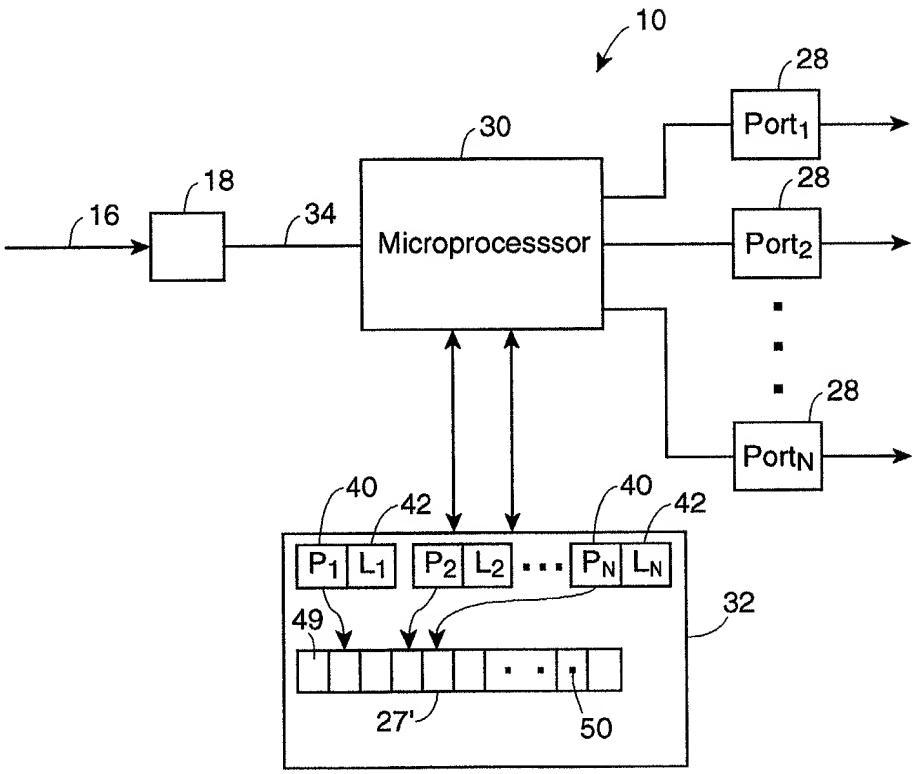


Figure 3B

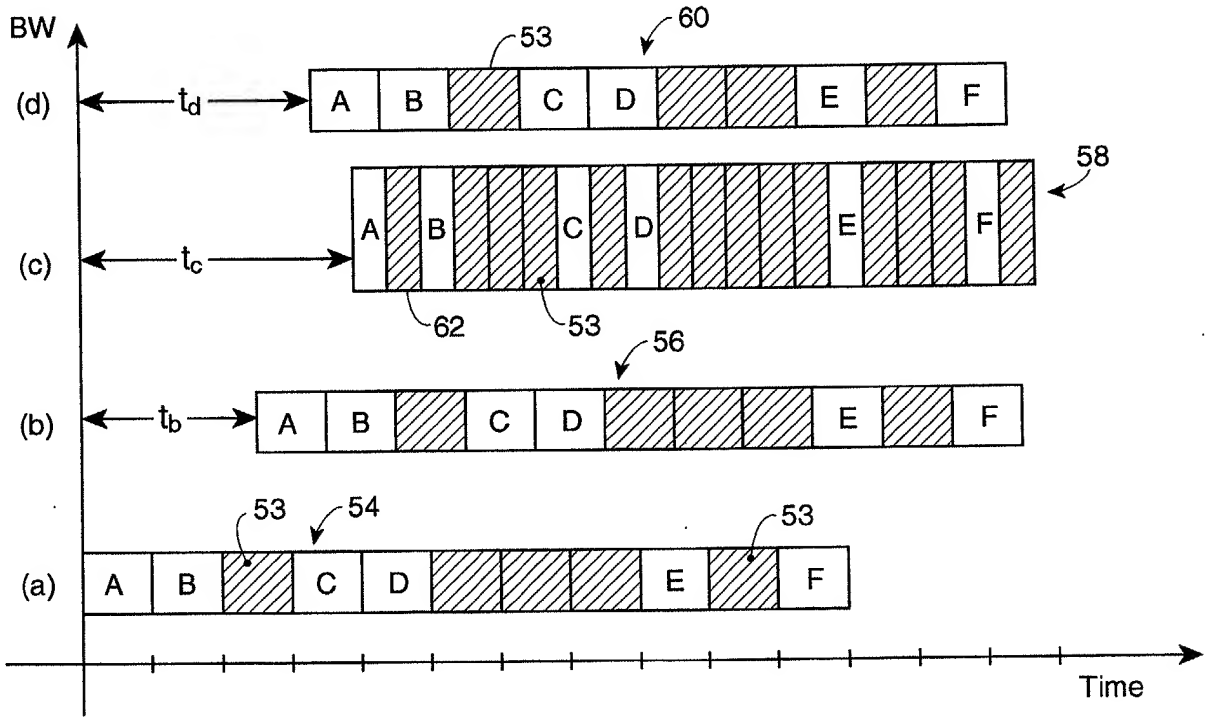


Figure 4

DECLARATION
Utility Application

DOCKET INFORMATION
53921/56

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **CELL STREAM REPLICATING DEVICE**, the specification of which

Check One

☑ is attached hereto.

☐ was filed on _____ as

Application Serial No._____

and was amended on_____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a). I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Application Number	Country	Date of Filing	Priority Yes✓	Claimed No✓
2,243,680	**Canada**	**July 22, 1998**	**X**	

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

Application Number	Date of Filing	Status — Patented, Pending or Abandoned

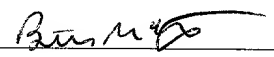
201	FULL NAME OF INVENTOR **FIRST** Name: **Brian**	Middle Initial(s): **E.**	**LAST** Name: **McBride**	
	RESIDENCE & CITIZENSHIP City: **Canadian**	State or Foreign Country: **Canada**	Country of Citizenship: **Canada**	
	POST OFFICE ADDRESS Post Office Address: **240 Castlefrank Road**	City: **Kanata**	State or Country: **Ontario, Canada**	Zip Code: **K2L 1T5**

202	FULL NAME OF INVENTOR **FIRST** Name:	Middle Initial(s):	**LAST** Name:	
	RESIDENCE & CITIZENSHIP City:	State or Foreign Country:	Country of Citizenship:	
	POST OFFICE ADDRESS Post Office Address:	City:	State or Country:	Zip Code:

203	FULL NAME OF INVENTOR **FIRST** Name:	Middle Initial(s):	**LAST** Name:	
	RESIDENCE & CITIZENSHIP City:	State or Foreign Country:	Country of Citizenship:	
	POST OFFICE ADDRESS Post Office Address:	City:	State or Country:	Zip Code:

204	FULL NAME OF INVENTOR **FIRST** Name:	Middle Initial(s):	**LAST** Name:	
	RESIDENCE & CITIZENSHIP City:	State or Foreign Country:	Country of Citizenship:	
	POST OFFICE ADDRESS Post Office Address:	City:	State or Country:	Zip Code:

I further declare that all statements made herein of may own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor **201** 	Signature of Inventor **203**
Date Jan 27 1995	Date
Signature of Inventor **202**	Signature of Inventor **204**
Date	Date

Signatures should conform to names as presented at 201 *et seq.* above.

POWER OF ATTORNEY

DOCKET INFORMATION
53921/56

MCBRIDE, Brian E., owner(s) of the application for United States Letters of Patent for **CELL STREAM REPLICATING DEVICE**,

by **MCBRIDE, Brian E.** _____
(Inventors)

☑ executed on even date herewith or

☐ having Serial No. _____, filed _____
_, 19_____,

do(es) hereby appoint as attorneys of record with full power of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith Brian W. Gray (Registration No. 30,017); Sheldon Burshtein (Registration No. 32,851); John C. Hunt (Registration No. 36,424); Alfred A. Macchione (Registration No. 40,333); Kenneth L. Bousfield (Registration No. 40,460); Alexander Porat (Registration No. 43-372); George E. Fisk (22,243); Terry L. Leier (41,554)

Send Correspondence to:	**Blake Cassels & Graydon** **Intellectual Property Group** **Box 25, Commerce Court West** **Toronto, ON**	Direct Telephone Calls to: Alex Porat (416) 863-2731

I , the undersigned, declare that I am the (an) owner of the above-identified application or, if the owner is a corporation, partnership or other association, I am authorized to make this appointment on behalf of the owner and I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full Name of Individual Owner	**MCBRIDE, Brian E.**
Post Office Address	**240 Castlefrank Road, Kanata, Ontario, K2L 1T5, Canada**
Signature of Owner	Date Jan 27 1999

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